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10CS74

Seventh Semester B.E. Degree Examination, June/July 2015
Advanced Computer Architectures

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Define instruction set architecture (ISA). Explain seven dimensions of an ISA. **(08 Marks)**

b. Briefly explain the Amdahl's law. **(06 Marks)**

c. Suppose that we want to enhance the processor used for web serving. The new processor is 10 times faster on computation in the web serving application than the original processor. Assuming that the original processor is busy with computation 40% of the time and is waiting for I/O 60% of the time, what is the overall speedup gained by incorporating the enhancement. **(06 Marks)**

2 a. With a neat diagram, explain the classic five stage pipeline for a RISC processor. **(10 Marks)**

b. Explain different techniques in reducing pipeline branch penalties. **(10 Marks)**

3 a. Define instruction level parallelism. Explain data dependencies and different types of data hazards with examples. **(08 Marks)**

b. What is correlating predictors? Explain with example. **(04 Marks)**

c. Explain Tomasulo's algorithm, sketching the basic structure of a MIPS floating point unit. **(08 Marks)**

4 a. Explain the basic VLIW approach for exploiting ILP, using multiple issues. **(08 Marks)**

b. Explain branch target buffer with neat diagram. **(06 Marks)**

c. What are the issues involved in implementation of speculation? Explain register renaming approach. **(06 Marks)**

PART – B

5 a. Explain the different taxonomy of parallel architecture. **(06 Marks)**

b. To achieve a speedup of 80 with 100 processors what fraction of original computation can be sequential? **(06 Marks)**

c. Explain the snooping, with respect to cache – coherence protocol. **(08 Marks)**

6 a. Briefly explain six basic cache optimization methods. **(12 Marks)**

b. With a neat diagram, explain the translation buffer of fast address translation. **(08 Marks)**

7 a. Which are the major categories of advanced optimizations of cache performance? Explain any one in detail. **(12 Marks)**

b. Explain DRAM memory technology with its basic organization. **(08 Marks)**

8 a. Explain in detail, the hardware support for preserving exception behaviour during speculation. **(10 Marks)**

b. Explain the architecture of IA64 intel processor and also prediction and speculation support provided. **(10 Marks)**

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